DRONACHARYA
College of Engineering

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department: Electronics and Communication Engineering

Academic Session: 2017-18 (Jan-June 2018)

Lesson Plan for the Semester started w.e.f 08.01.2018

Subject with code: Digital System Design (EE-310-F)

Name of Faculty with designation : Ashish Gambhir (Assistant Professor)

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Academic activity	Test / assignment
January	**10-Jan-18**	**VI-ECE**	1	Importance of CAD Design Tools, Review of Digital Circuits and Systems	……	**Assignment of 2 Ques. Given**
January	**12-Jan-18**	**VI-ECE**	1	Review of Digital Systems		**Assignment of 2 Ques. Given**
January	**17-Jan-18**	**VI-ECE**	1	Introduction to HDL and its difference from other Hardware Languages		**Assignment of 2 Ques. Given**
January	**19-Jan-18**	**VI-ECE**	1	Data Objects & Classes in VHDL		**Assignment of 2 Ques. Given**
January	**24-Jan-18**	**VI-ECE**	1	Data Types in VHDL		**Assignment of 2 Ques. Given**
January	**24-Jan-18**	**VI-ECE**	1	Operators and Operator Overloading in VHDL, Types of Delays		**Assignment of 2 Ques. Given**
January	**31-Jan-18**	**VI-ECE**	1	Demonstration of First Program in VHDL		**Assignment of 2 Ques. Given**
January	**31-Jan-18**	**VI-ECE**	1	Entity and Architecture Declaration		**Assignment of 2 Ques. Given**
February	**2-Feb-18**	**VI-ECE**	1	Introduction to behavioural, dataflow and structural models.		**Assignment of 2 Ques. Given**
February	**7-Feb-18**	**VI-ECE**	2	Assignment statements, sequential statements and process		**Assignment of 2 Ques. Given**
February	**9-Feb-18**	**VI-ECE**	2	Conditional statements, case statement Array and loops		**Assignment of 2 Ques. Given**
February	**21-Feb-18**	**VI-ECE**	2	Resolution functions, Packages and Libraries, concurrent statements		**Assignment of 2 Ques. Given**
February	**21-Feb-18**	**VI-ECE**	2	Application of Functions and Procedures		**Assignment of 2 Ques. Given**
February	**23-Feb-18**	**VI-ECE**	2	Structural Modelling, component declaration		**Assignment of 2 Ques. Given**
February	**23-Feb-18**	**VI-ECE**	2	Structural layout and generics		**Assignment of 2 Ques. Given**
February	**28-Feb-18**	**VI-ECE**	3	VHDL Models and Simulation of combinational circuits of Mux and Demux		**Assignment of 2 Ques. Given**

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Academic activity	Test / assignment
March	**7-Mar-18**	**VI-ECE**	3	VHDL Models and Simulation of combinational circuits of Encoders, Decoder		**Assignment of 2 Ques. Given**
March	**9-Mar-18**	**VI-ECE**	3	VHDL Models and Simulation of combinational circuits of Code Converters		**Assignment of 2 Ques. Given**
March	**14-Mar-18**	**VI-ECE**	3	VHDL Models and Simulation of combinational circuits of Comparators		**Assignment of 2 Ques. Given**
March	**16-Mar-18**	**VI-ECE**	3	Implementation of Sequential Circuits - Shift Registers, Counters		**Assignment of 2 Ques. Given**
March	**28-Mar-18**	**VI-ECE**	4	Basic components of a computer, specifications		**Assignment of 2 Ques. Given**
March	**30-Mar-18**	**VI-ECE**	4	Architecture of a simple microcomputer system		**Assignment of 2 Ques. Given**
April	**4-Apr-18**	**VI-ECE**	4	Implementation of a simple microcomputer system using VHDL		**Assignment of 2 Ques. Given**
April	**6-Apr-18**	**VI-ECE**	4	Progr ammable logic devices : ROM, PLAs, PALs		**Assignment of 2 Ques. Given**
April	**11-Apr-18**	**VI-ECE**	4	GAL, PEEL		**Assignment of 2 Ques. Given**
April	**13-Apr-18**	**VI-ECE**	4	CPLDs and FPGA		**Assignment of 2 Ques. Given**
April	**25-Apr-18**	**VI-ECE**	4	Design implementation using CPLDs and FPGAs		**Assignment of 2 Ques. Given**